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**CA Lab09 Report**

**TASK 1:**

**module Program\_Counter**

(

input clk, reset,

input[63:0] PC\_In,

output reg [63:0] PC\_Out

);

always@(posedge clk)

begin

if (reset)

PC\_Out = 0;

else

PC\_Out = PC\_In;

end

endmodule

**TASK 2:**

**module Adder**

(

input[63:0] a, b,

output reg[63:0] out

);

always@(\*)

begin

out = a + b;

end

endmodule

**TASK 3:**

Using PC and Adder modules from task1 and task2 resp. and Instruction Memory module from lab8

**module Instruction\_Memory**

(

input[63:0] Inst\_Address,

output reg[31:0] Instruction

);

reg[7:0] Inst\_Mem[15:0];

//initialize acc to fig:8.3

initial

begin

Inst\_Mem[0] = 8'b10000011;

Inst\_Mem[1] = 8'b00110100;

Inst\_Mem[2] = 8'b00000101;

Inst\_Mem[3] = 8'b00001111;

Inst\_Mem[4] = 8'b10110011;

Inst\_Mem[5] = 8'b10000100;

Inst\_Mem[6] = 8'b10011010;

Inst\_Mem[7] = 8'b00000000;

Inst\_Mem[8] = 8'b10010011;

Inst\_Mem[9] = 8'b10000100;

Inst\_Mem[10] = 8'b00010100;

Inst\_Mem[11] = 8'b00000000;

Inst\_Mem[12] = 8'b00100011;

Inst\_Mem[13] = 8'b00111000;

Inst\_Mem[14] = 8'b10010101;

Inst\_Mem[15] = 8'b00001110;

end

always@(\*)

begin

//concatenate Inst\_Mem[Inst\_Address+3:Inst\_Address] as output Instruction

assign Instruction = { Inst\_Mem[Inst\_Address+3], Inst\_Mem[Inst\_Address+2] ,Inst\_Mem[Inst\_Address+1], Inst\_Mem[Inst\_Address]};

end

endmodule

**module Instruction\_Fetch**

(

input clk, reset,

output[31:0] Instruction

);

wire[63:0] pc\_wire;

wire[63:0] add\_out;

Program\_Counter PC

(

.clk(clk),

.reset(reset),

.PC\_In(add\_out),

.PC\_Out(pc\_wire)

);

Instruction\_Memory ins\_mem

(

.Inst\_Address(pc\_wire),

.Instruction(Instruction)

);

Adder adder

(

.a(pc\_wire),

.b(64'd4),

.out(add\_out)

);

endmodule

**module tb**

(

);

reg clk, reset;

wire [31:0] Instruction;

Instruction\_Fetch instruction\_fetch

(

.clk(clk),

.reset(reset),

.Instruction(Instruction)

);

initial

begin

clk = 0;

reset = 1;

#10 reset = ~reset;

end

always

#5 clk = ~clk;

endmodule

